THE EQUATIONS OF THE IDEAL LATCHES

Şerban E. Vlad

The Computers Department Oradea City Hall, Oradea

Abstract

The latches are simple circuits with feedback from the digital electrical engineering. We have included in our work the C element of Muller, the RS latch, the clocked RS latch, the D latch and also circuits containing two interconnected latches: the edge triggered RS flip-flop, the D flip-flop, the JK flip-flop, the T flip-flop. Our purpose is to model by equations the previous circuits, considered to be ideal, i.e. non-inertial. The technique of analysis is the pseudoboolean differential calculus.

Keywords: latch, flip-flop, pseudo-boolean equations.

1. LATCHES, THE GENERAL EQUATION

$\mathbb{B} = \{0, 1\}$ is the Boole algebra with two elements. The (normal) signals are, by definition, the functions $x : \mathbb{R} \rightarrow \mathbb{B}$ of the form

$$x(t) = x(\tau_0 - 0) \cdot \varphi_{(-\infty, \tau_0)}(t) \oplus x(\tau_0) \cdot \varphi_{[\tau_0, \tau_1)}(t) \oplus x(\tau_1) \cdot \varphi_{[\tau_1, \tau_2)}(t) \oplus ..., $$

where $\mathbb{R}$ is the time set, $\varphi(\cdot) : \mathbb{R} \rightarrow \mathbb{B}$ is the characteristic function and $0 \leq \tau_0 < \tau_1 < \tau_2 < ...$ is an unbounded sequence. The equations of the (ideal) latches consist in the next system

$$x(t) \cdot x = x(t) \cdot u, \quad x(t) \cdot \overline{x} = x(t) \cdot v, \quad u \cdot v = 0,$$  \hspace{1cm} (1)

where $u, v, x$ are signals and $x$ is the unknown. The last equation of the system is called the admisibility condition (of the inputs). In order to solve the system (1.1) we associate with the functions $u, v$ the next sets $U_{2k}, V_{2k+1}$ and respectively numbers $t_k$:

$$U_0 = \{t | u(t-0) \cdot u(t) = 1\}, \quad t_0 = \min U_0$$

$$V_1 = \{t | v(t-0) \cdot v(t) = 1, t > t_0\}, \quad t_1 = \min V_1$$

$$U_2 = \{t | u(t-0) \cdot u(t) = 1, t > t_1\}, \quad t_2 = \min U_2$$

$$V_3 = \{t | v(t-0) \cdot v(t) = 1, t > t_2\}, \quad t_3 = \min V_3...$$

and the next inclusions, respectively inequalities are true:

$$U_0 \supset U_2 \supset U_4 \supset ... \supset V_1 \supset V_3 \supset V_5 \supset ..., \quad 0 \leq t_0 < t_1 < t_2 < ...$$

For each of $U_{2k}$ $(V_{2k+1})$ we have the possibilities:
- it is empty. Then \( t_{2k} (t_{2k+1}) \) is undefined and all \( U_{2k}, V_{2k+1}, t_k \) of higher rank are undefined;
- it is non-empty, finite or infinite. \( t_{2k} (t_{2k+1}) \) is defined.
If \( U_{2k} (V_{2k+1}) \) are defined for all \( k \in \mathbb{N} \), then the sequence \( (t_k) \) is unbounded.

A similar discussion is related with the sets \( V'_{2k}, U'_{2k+1} \) and respectively numbers \( t'_{k} \):
\[
\begin{align*}
V'_0 &= \{ t|v(t-0) \cdot v(t) = 1 \}, & t'_0 &= \min V'_0 \\
U'_1 &= \{ t|u(t-0) \cdot u(t) = 1, t > t'_0 \}, & t'_1 &= \min U'_1 \\
V'_2 &= \{ t|v(t-0) \cdot v(t) = 1, t > t'_1 \}, & t'_2 &= \min V'_2 \\
U'_3 &= \{ t|u(t-0) \cdot u(t) = 1, t > t'_2 \}, & t'_3 &= \min U'_3...
\end{align*}
\]

For solving the system (1.1) we note that the unbounded sequence \( 0 \leq t'_0 < t'_1 < t'_2 < ... \) exists with the property that \( u, v, x \) are constant in each of the intervals \( (-\infty, t'_0), [t'_0, t'_1), [t'_1, t'_2), ... \) where the first two equations of (1.1) take one of the forms
\[
\begin{align*}
\overline{x(t-0) \cdot x(t)} &= \overline{x(t-0)} \cdot \overline{x(t)} = 0, & (2) \\
\overline{x(t-0) \cdot x(t)} &= 0, \overline{x(t-0) \cdot x(t)} = \overline{x(t-0)}, & (3) \\
\overline{x(t-0) \cdot x(t)} &= 0, \overline{x(t-0) \cdot x(t)} = 0, & (4)
\end{align*}
\]
as \( u(t), v(t) \) are equal to 1,0;0,1;0,0 in those intervals. The solutions are written in Table 1.

<table>
<thead>
<tr>
<th>( t \in (-\infty, t'_0) )</th>
<th>( t \in [t'<em>k, t'</em>{k+1}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( u(t) = 1, v(t) = 0 )</td>
<td>( x(t) = 1 )</td>
</tr>
<tr>
<td>( u(t) = 0, v(t) = 1 )</td>
<td>( x(t) = 0 )</td>
</tr>
<tr>
<td>( u(t) = v(t) = 0 )</td>
<td>( x(t) = x(t'_k - 0) )</td>
</tr>
</tbody>
</table>

**Table 1.**

**Theorem 1.1.** *Equation (1.1) is equivalent with the equation*
\[
\overline{x(t-0) \cdot u(t) \cdot v(t) \cup \overline{x(t)} \cdot u(t) \cdot v(t)} \cup \overline{x(t-0) \cdot x(t) \cdot u(t) \cdot v(t)} = 1. \tag{5}
\]

*Proof* The proof is elementary and it is omitted. \[\Box\]

Equation (1.5) contains three exclusive possibilities: \( x(t) \cdot u(t) \cdot \overline{v(t)} = 1, \overline{x(t)} \cdot \overline{u(t)} \cdot v(t) = 1, \) respectively \( \overline{x(t-0) \cdot x(t)} \cdot u(t) \cdot v(t) = 1 \) equivalent with (1.2), (1.3), (1.4).

Let us solve the system (1.1).
The equations of the ideal latches

Case a) \( u(0-0) = 0, v(0-0) = 0 \). \( x(0-0) = 0 \) and \( x(0-0) = 1 \) are both possible. In order to make a distinction between the two solutions of (1.1) corresponding to the initial value 0, respectively to the initial value 1 we shall denote them by \( x \) and \( x' \), respectively.

a.i) \( x(0-0) = 0 \). a.i.1) \( U_0 = \emptyset \), the solution of (1.1) is \( x(t) = 0 \), a.i.2) \( U_0 \neq \emptyset \) and \( \exists \varepsilon > 0, x(t) = \varphi_{[t_0, \infty)}(t) \) for \( t < t_0 + \varepsilon \). This fact results by solving (1.4) for \( t < t_0 \) and then (1.2) followed perhaps by a finite sequence of (1.4), (1.2), (1.4)\( \ldots \) in some interval \([t_0, t_0 + \varepsilon)\). Furthermore a.i.2.1) \( V_1 = \emptyset \), the solution of (1.1) is \( x(t) = \varphi_{[t_0, \infty)}(t) \). a.i.2.2) \( V_1 \neq \emptyset \) and \( \exists \varepsilon > 0, x(t) = \varphi_{[t_0,t_1)}(t) \) for \( t < t_1 + \varepsilon \). In some interval \([t_1, t_1 + \varepsilon)\), we solved (1.3) followed perhaps by a finite sequence of (1.4), (1.3), (1.4)\( \ldots \) a.i.2.2.1) \( U_2 = \emptyset \), the solution of (1.1) is \( x(t) = \varphi_{[t_0,t_1)}(t) \), a.i.2.2.2) \( U_2 \neq \emptyset \) and \( \exists \varepsilon > 0, x(t) = \varphi_{[t_0,t_1)}(t) \oplus \varphi_{[t_2, \infty)}(t) \) for \( t < t_2 + \varepsilon \). a.i.2.2.2.1) \( V_3 = \emptyset \), the solution of (1.1) is \( x(t) = \varphi_{[t_0,t_1)}(t) \oplus \varphi_{[t_2, \infty)}(t) \), a.i.2.2.2.2) \( V_3 \neq \emptyset \)\( \ldots \) a.ii) \( x'(0-0) = 1 \), a.ii.1) \( V_0' = \emptyset \), the solution of (1.1) is \( x'(t) = 1 \), a.ii.2) \( V_0' \neq \emptyset \), \( \exists \varepsilon > 0, x'(t) = \varphi_{(-\infty, t_0')} (t) \) for all \( t < t_0' + \varepsilon \), a.ii.2.1) \( U_1' = \emptyset \), the solution of (1.1) is \( x'(t) = \varphi_{(-\infty, t_0')} (t) \oplus \varphi_{[t_1', \infty)}(t) \) for all \( t < t_1' + \varepsilon \)\( \ldots \)

In figs. 1 and 2 we have drawn the solutions \( x, x' \) corresponding to case a) in the situation when \( t_0 < t_0' \), respectively when \( t_0 > t_0' \) (the equality \( t_0 = t_0' \) is impossible, because it implies \( u(t_0) = v(t_0) = 0 \), contradiction with (1.1)). We note the fact that \( x|_{[t_0, \infty)} = x'|_{[t_0, \infty)} \), respectively \( x'|_{[t_0, \infty)} = x|_{[t_0', \infty)} \). Thus after the first common value of the (distinct) solutions \( x, x' \) they coincide

\[ x|_{[t_0, \infty)} = x'|_{[t_0, \infty)} \]

Case b) \( u(0-0) = 1, v(0-0) = 0 \), the only possibility is \( x(0-0) = 1 \), b.1) \( V_0' = \emptyset \), the solution of (1.1) is \( x(t) = 1 \), b.2) \( V_0' \neq \emptyset \), \( \exists \varepsilon > 0, x(t) = \varphi_{(-\infty, t_0')} (t) \) for all \( t < t_0' + \varepsilon \)\( \ldots \)

Case c) \( u(0-0) = 0, v(0-0) = 1 \), the only possibility is \( x(0-0) = 0 \), c.1) \( U_0 = \emptyset \), the solution of (1.1) is \( x(t) = 0 \), c.2) \( U_0 \neq \emptyset \), \( \exists \varepsilon > 0, x(t) = \varphi_{[t_0, \infty)}(t) \) for \( t < t_0 + \varepsilon \)\( \ldots \)

We have proved the next

**Theorem 1.2.** If \( u(t) = v(t) = 0 \), the system (1.1) has two solutions \( x(t) = 0 \) and \( x(t) = 1 \). If \( u(0-0) = v(0-0) = 0 \) but \( \exists t > 0, u(t) \cup v(t) = 1 \), then (1.1)
has two distinct solutions corresponding to $x(0^-) = 0$ and $x(0^-) = 1$, that become equal at the first time instant $t > 0$ when $u(t) \cup v(t) = 1$. If $u(0^-) \cup v(0^-) = 1$, then the solution is unique.

2. C ELEMENT

We call the equations of the C element of Muller any of the next equivalent statements

$$
\begin{align}
&x(t-0) \cdot x(t) = x(t-0) \cdot u(t) \cdot v(t) \\
&x(t-0) \cdot \overline{x(t)} = x(t-0) \cdot \overline{u(t)} \cdot \overline{v(t)}
\end{align}
$$

(6)

and respectively

$$
\begin{align}
x(t) \cdot u(t) \cdot v(t) &\cup x(t) \cdot \overline{u(t)} \cdot v(t) \cup \\
(x(t-0) \cdot x(t) \cup x(t-0) \cdot x(t)) \cdot (u(t) \cdot v(t) \cup u(t) \cdot \overline{v(t)}) &= 1
\end{align}
$$

(7)

3. RS LATCH

The equations of the RS latch are given by

$$
\overline{Q(t-0)} \cdot Q(t) = Q(t-0) \cdot \overline{S(t)}, Q(t-0) \cdot \overline{Q(t)} = Q(t-0) \cdot \overline{R(t)}, R(t) \cdot S(t) = 0
$$

and equivalently by

$$
\begin{align}
&Q(t) \cdot \overline{R(t)} \cdot S(t) \cup Q(t) \cdot R(t) \cdot \overline{S(t)} \cup \\
&\cup (Q(t-0) \cdot Q(t) \cup Q(t-0) \cdot Q(t)) \cdot \overline{R(t)} \cdot \overline{S(t)} = 1
\end{align}
$$

(9)
In (3.1), (3.2) \( R, S, Q \) are signals. \( R, S \) are called inputs: the reset input and the set input and \( Q \) is the state, the unknown relative to which the equations are solved. These equations coincide with (1.1) and (1.5) but the notations are different and traditional. To conclude with, we make the following statements related to equation (3.2). At the RS latch, \( Q(t) = 1 \) if \( R(t) = 0, S(t) = 1; Q(t) = 0 \) if \( R(t) = 1, S(t) = 0; \) and \( Q(t) = Q(t - 0), Q \) keeps its previous value if \( R(t) = 0, S(t) = 0. \)

4. CLOCKED RS LATCH

The equivalent statements

\[
\begin{align*}
Q(t - 0) \cdot Q(t) &= Q(t - 0) \cdot S(t) \cdot C(t), \\
Q(t - 0) \cdot \overline{Q(t)} &= Q(t - 0) \cdot R(t) \cdot C(t), \\
S(t) \cdot C(t) &= 0.
\end{align*}
\]

\[
C(t) \cdot (Q(t) \cdot R(t)) \cdot S(t) \cup \overline{Q(t)} \cdot R(t) \cdot \overline{S(t)} \cup \\
\cup (Q(t - 0) \cdot \overline{Q(t)} \cup Q(t - 0) \cdot Q(t)) \cdot \overline{R(t)} \cdot \overline{S(t)} \cup \\
\cup \overline{C(t)} \cdot (Q(t - 0) \cdot \overline{Q(t)} \cup Q(t - 0) \cdot Q(t)) = 1
\]

are called the equations of the clocked RS latch. \( R, S, C, Q \) are signals: the reset, the set and the clock input, the state respectively. The equations (4.1), (4.2) follow from (1.1) and (1.5), where \( u(t) = S(t) \cdot C(t), v(t) = R(t) \cdot C(t). \) The clocked RS latch behaves like an RS latch when \( C(t) = 1 \) and keeps the state constant \( Q(t) = Q(t - 0) \) when \( C(t) = 0. \)
5. D LATCH

We call the equations of the D latch any of the next equivalent statements

\[
\begin{align*}
Q(t-0) \cdot Q(t) &= Q(t-0) \cdot D(t) \cdot C(t) \\
Q(t-0) \cdot Q(t) &= Q(t-0) \cdot D(t) \cdot C(t)
\end{align*}
\]

(11)

and respectively

\[
C(t) \cdot (\overline{Q(t)} \cdot \overline{D(t)} \cup Q(t) \cdot D(t)) \cdot \overline{C(t)} \cdot (\overline{Q(t-0)} \cdot Q(t) \cup Q(t-0) \cdot Q(t)) = 1
\]

(12)

\[D, C, Q\] are signals: the data input \(D\), the clock input \(C\) and the state \(Q\). On one hand, from (5.1) it is seen the satisfaction of the admissibility condition of the inputs. On the other hand, (5.1), (5.2) follow from the equations of the clocked RS latch (4.1), (4.2) where \(R = S \cdot C\) and we have used the traditional notation \(D\) for the data input, instead of \(S\).

If \(C(t) = 1\), the D latch it \(Q(t) = D(t)\); if \(C(t) = 0\), \(Q\) is constant.

6. EDGE TRIGGERED RS FLIP-FLOP

Any of the equivalent statements

\[
\begin{align*}
\overline{P(t-0)} \cdot P(t) &= \overline{P(t-0)} \cdot S(t) \cdot C(t) \\
P(t-0) \cdot P(t) &= P(t-0) \cdot R(t) \cdot C(t) \\
R(t) \cdot S(t) \cdot C(t) &= 1 \\
\overline{Q(t-0)} \cdot Q(t) &= Q(t-0) \cdot P(t) \cdot \overline{C(t)} \\
Q(t-0) \cdot Q(t) &= Q(t-0) \cdot P(t) \cdot C(t)
\end{align*}
\]

(13)

and respectively
The equations of the ideal latches

\[
C(t) \cdot (Q(t) - Q(t-0) \cup Q(t-0) \cdot Q(t)) \cdot (P(t) \cdot R(t) \cdot S(t) \cup \\
P(t) \cdot R(t) \cdot \overline{S(t)} \cup (\overline{P(t)} \cdot \overline{P(t)} \cup P(t-0) \cdot P(t)) \cdot \overline{R(t)} \cdot \overline{S(t)}) \cup \\
\overline{C(t)} \cdot (Q(t) \cdot \overline{P(t-0)} \cdot \overline{P(t)} \cup Q(t) \cdot P(t-0) \cdot P(t)) = 1
\]

is called the equation of the edge triggered RS flip-flop. \(R, S, C, P, Q\) are signals: the reset input \(R\), the set input \(S\), the clock input \(C\), the next state \(P\) and the state \(Q\). In (6.1), (6.2) the signals \(R, S, C, P\) and \(P, C, Q\) satisfy the equations of a clocked RS latch and of a D latch and (6.2) represents the term by term product of (4.2) by (5.2) written with these variables. The two latches are called master and slave. The name of edge triggered RS flip-flop refers to the fact that \(Q(t)\) is constant at all time instances except \(C(t-0) \cdot \overline{C(t)} = 1\), when

\[
Q(t) = P(t-0) = \begin{cases} 
1, & \text{if } R(t-0) = 0, S(t-0) = 1 \\
0, & \text{if } R(t-0) = 1, S(t-0) = 0
\end{cases}
\]

this is the so called falling edge of the clock input.

7. D FLIP-FLOP

We call the equations of the D flip-flop any of the next equivalent conditions

\[
\begin{align*}
P(t-0) \cdot P(t) &= P(t-0) \cdot D(t) \cdot C(t) \\
P(t-0) \cdot \overline{P(t)} &= P(t-0) \cdot \overline{D(t)} \cdot C(t) \\
Q(t-0) \cdot Q(t) &= Q(t-0) \cdot P(t) \cdot C(t) \\
Q(t-0) \cdot \overline{Q(t)} &= Q(t-0) \cdot \overline{P(t)} \cdot \overline{C(t)}
\end{align*}
\]

and respectively

\[
C(t) \cdot (Q(t-0) \cdot \overline{Q(t)} \cup Q(t-0) \cdot Q(t)) \cdot (\overline{P(t)} \cdot \overline{D(t)} \cup P(t) \cdot D(t)) \cup \\
\overline{C(t)} \cdot (Q(t) \cdot \overline{P(t-0)} \cdot \overline{P(t)} \cup Q(t) \cdot P(t-0) \cdot P(t)) = 1
\]

\(D, C, P, Q\) are signals, called: the data input \(D\), the clock input \(C\), the next state \(P\) and the state \(Q\). We note that the equations of the D flip-flop represent the special case of edge triggered RS flip-flop when \(R = S \cdot C\) and \(S\) was
denoted by $D$. The D flip-flop has the state $Q$ constant except for the time instants when $C(t-0) \cdot \overline{C(t)} = 1$; then $Q(t) = D(t-0)$.

8. **JK FLIP-FLOP**

The equivalent statements

\[
\begin{align*}
  P(t-0) \cdot P(t) &= P(t-0) \cdot J(t) \cdot Q(t) \cdot C(t) \\
  P(t-0) \cdot \overline{P(t)} &= P(t-0) \cdot K(t) \cdot Q(t) \cdot C(t) \\
  Q(t-0) \cdot Q(t) &= Q(t-0) \cdot P(t) \cdot C(t) \\
  Q(t-0) \cdot \overline{Q(t)} &= Q(t-0) \cdot \overline{P(t)} \cdot C(t)
\end{align*}
\]

(17)

and

\[
C(t) \cdot (Q(t-0) \cdot Q(t) \cup Q(t-0) \cdot Q(t)) \cdot (P(t) \cdot J(t) \cdot \overline{Q(t)} \cup \overline{P(t)} \cdot K(t) \cdot Q(t)) \cup
\]

\[
\cup (P(t-0) \cdot \overline{P(t)} \cup P(t-0) \cdot P(t)) \cdot (\overline{J(t)} \cdot K(t) \cup J(t) \cdot \overline{Q(t)} \cup Q(t) \cup K(t) \cdot Q(t) \cup)
\]

(18)

\[
\cup C(t) \cdot (Q(t) \cdot P(t-0) \cdot \overline{P(t)} \cup Q(t) \cdot P(t-0) \cdot P(t)) = 1
\]

are called the **equations of the JK flip-flop**. $J, K, C, P, Q$ are signals: the J input, the K input, the clock input C, the next state P and the state Q. The first two equations of (8.1) (modeling the master latch) coincide with the first two equations of the edge triggered RS flip-flop where $S(t) = J(t) \cdot Q(t)$, $R(t) = K(t) \cdot Q(t)$ and the last two equations of (8.1) (modeling the slave latch) coincide with the last two equations of the edge triggered RS flip-flop. We notice that the conditions of admissibility of the inputs of the master and of the slave latch are fulfilled. To be compared (8.2) and (6.2). The JK flip-flop is similar to the edge triggered flip-flop, for example $Q$ changes value only when $C(t-0) \cdot C(t) = 1$. Let $C(t) = 1$; because $Q(t) = Q(t-0)$, i.e. $Q$ is constant, in the union.
only one of \( P(t) \cdot J(t) \cdot Q(t) \cup \overline{P(t)} \cdot K(t) \cdot Q(t) \cup \\
\overline{P(t - 0)} \cdot \overline{P(t)} \cup P(t - 0) \cdot P(t) \cdot (\overline{J(t)} \cdot \overline{K(t)} \cup J(t) \cdot \overline{Q(t)} \cup K(t) \cdot Q(t)) \) \\

\( C(t) \cdot (Q(t - 0) \cdot \overline{Q(t)} \cup Q(t - 0) \cdot Q(t)) \cdot (P(t) \cdot J(t) \cdot \overline{Q(t)} \cup \overline{P(t)} \cdot K(t) \cdot Q(t) \cup \\
\overline{P(t)} \cdot J(t) \cdot \overline{Q(t)} \cup P(t) \cdot \overline{K(t)} \cdot Q(t)) \cup \\
\overline{C(t)} \cdot (Q(t) \cdot \overline{P(t - 0)} \cdot \overline{P(t)} \cup Q(t) \cdot P(t - 0) \cdot P(t)) = 1 \)

Equations (8.2) and (8.3) have similarities and sometimes the equation of the JK flip-flop is considered to be (8.3).

9. **T FLIP-FLOP**

The next equivalent statements \( \overline{P(t - 0)} \cdot P(t) = \overline{P(t - 0)} \cdot \overline{Q(t)} \cdot C(t), P(t - 0) \cdot \overline{P(t)} = P(t - 0) \cdot Q(t) \cdot C(t) \) \\
\( \overline{Q(t - 0)} \cdot Q(t) = \overline{Q(t - 0)} \cdot P(t) \cdot \overline{C(t)}, Q(t - 0) \cdot \overline{Q(t)} = Q(t - 0) \cdot \overline{P(t)} \cdot \overline{C(t)} \) \\

respectively

\( C(t) \cdot (\overline{Q(t - 0)} \cdot \overline{Q(t)} \cdot P(t) \cup Q(t - 0) \cdot Q(t) \cdot \overline{P(t)}) \cup \\
\overline{C(t)} \cdot (Q(t) \cdot \overline{P(t - 0)} \cdot \overline{P(t)} \cup Q(t) \cdot P(t - 0) \cdot P(t)) = 1 \)

are called the equations of the T flip-flop. \( C, P, Q \) are signals: the clock input, the next state and the state. The conditions of admissibility of the inputs are fulfilled for the first two and for the last two equations from (9.1) (the master and the slave latch). At each falling edge \( C(t - 0) \cdot \overline{C(t)} = 1 \) of the clock input, the state \( Q \) of the T flip-flop toggles to its complementary value, otherwise it is constant. The equations of the T flip-flop represent the next special cases: in the equations of the edge triggered RS flip-flop, \( S(t) = \overline{Q(t)}, R(t) = Q(t); \)
in the equations of the D flip-flop $D(t) = \overline{Q(t)}$; in the equations of the JK flip-flop (any of (9.2), (9.3)) $J(t) = 1, K(t) = 1$.

![Fig. 17. The T flip-flop circuit.](image1)

![Fig. 18. The symbol of the T flip-flop.](image2)

10. CONCLUSIONS

Digital electrical engineering is a non-formalized theory, where the latches are fundamental circuits. In our work we have given the general form of the equations that model the ideal latches, together with the theorem that characterizes the existence and the uniqueness of the solution. Furthermore, we have shown particular forms taken by this system of equations in the case of the most well-known latches and flip-flops. The bibliography dedicated to the latches is rich and descriptive (non-formalized). We quoted references which were a source of inspiration creating some order in our thoughts.

A possibility of continuing the present ideas is that of considering models of inertial latches, for example we can replace (1.1) by

$$\bigcap_{\xi \in [t-d, t]} u(\xi) \cdot x(t-0) \cdot x(t) = x(t-0) \cdot \bigcap_{\xi \in [t-d, t]} v(\xi), \bigcap_{\xi \in [t-d, t]} u(\xi) \cdot \bigcap_{\xi \in [t-d, t]} v(\xi) = 0,$$

where $d > 0$. We remark that this model replaces $u$ (of $v$) by

$$\bigcap_{\xi \in [t-d, t]} u(\xi)$$

we meant that the 1 value of $u$ (of $v$) continues to produce the switch of $x$ from 0 to 1 (from 1 to 0), but this happens only if it is persistent, i.e. if it lasts at least $d$ time units.

References